Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-21. (canceled)

22. (currently amended) A programmable array module comprising:

at least a first integrated circuit functional element including a field programmable gate array; and

at least a second integrated circuit functional element including a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit functional element,

wherein said field programmable gate array is programmable as a processing element, and wherein said memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element.

23-31. (canceled)

32. (currently amended) A programmable array module comprising:

at least a first integrated circuit functional element including a field programmable gate array; and

at least a second integrated circuit functional element including a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit functional element, said first and second integrated circuit functional elements being coupled by a number of contact points distributed throughout the surfaces of said functional elements,

wherein said field programmable gate array is programmable as a processing element, and wherein said memory array is functional to accelerate reconfiguration of said field programmable gate array as a processing element.

33-36. (canceled)

37. (original) The programmable array module of claim 32 wherein said contact points are further functional to provide test stimulus from said field programmable gate array to said at least second integrated circuit functional element.

38. (original) The programmable array module of claim 32 further comprising:

at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements.

39. (original) The programmable array module of claim 38 wherein said third integrated circuit functional element includes another field programmable gate array.

40. (original) The programmable array module of claim 38 wherein said third integrated circuit functional element includes an I/O controller.

41. (original) A method of fabricating a programmable array module comprising:

forming at least a first integrated circuit functional element including a field programmable gate array and a plurality of metal pads on a base wafer;

forming a first epitaxial layer over the first integrated circuit functional element; and

forming at least a second integrated circuit functional element including a memory array in the first epitaxial layer, the second integrated circuit functional element having a plurality of metal pads, at least one of which is in electrical contact with the metal pads of the first integrated circuit functional element.

42. (original) The method of claim 41 further comprising forming a first layer of silicon dioxide on the surface of the first integrated circuit functional element.

43. (original) The method of claim 42 further comprising forming the first epitaxial layer on the surface of the first silicon dioxide layer.

44. (original) The method of claim 41 wherein forming the first epitaxial layer comprises forming a polysilicon layer.

45. (currently amended) The method of claim 41 further comprising etching through the first epitaxial layer so that an interconnection between the metal pads of the first and second integrated circuit functional elements is ~~can be~~ subsequently formed.

46. (original) The method of claim 45 further comprising etching through a first silicon dioxide layer on the surface of the first integrated circuit functional element.

47. (currently amended) The method of claim 41 further comprising forming a second epitaxial layer over the first epitaxial layer such that a third functional element is ~~can be~~ integrated with the first two functional elements.

48. (original) The method of claim 47 wherein forming the third functional element comprises forming an I/O controller, memory, FPGA, or microprocessor.

49. (original) The method of claim 47 further comprising forming a second silicon dioxide layer on the surface of the second epitaxial layer.

50. (original) The method of claim 47 wherein forming the second epitaxial layer comprises forming a polysilicon layer.

51. (currently amended) A method of fabricating a processor module comprising:

forming at least a first integrated circuit functional element including ~~such as~~ a microprocessor on a base wafer; and

using wafer processing techniques, forming at least a second integrated circuit functional element such as a field programmable gate array on the first integrated circuit functional element,

wherein forming the second integrated circuit functional element comprises forming an epitaxial layer.

52. (original) The method of claim 51 further comprising forming an electrical contact between at least one of a plurality of metal pads associated with the first integrated circuit functional element and at least one of a plurality of metal pads associated with the second integrated circuit functional element.

53. (canceled)

54. (currently amended) The method of claim 51 [[53]] wherein forming the epitaxial layer comprises forming a polysilicon layer.

55. (original) The method of claim 51 further comprising forming a silicon dioxide layer on a top surface of the first integrated circuit functional element.

56. (original) The method of claim 51 further comprising etching through the second integrated circuit functional element so that an electrical interconnection can be established between the first and second integrated circuit functional elements.

57. (original) The method of claim 51 further comprising forming a third functional element integrated with the first two functional elements using wafer processing techniques.

58. (original) The method of claim 57 wherein forming the third functional element comprises forming an epitaxial layer.

59. (original) The method of claim 58 wherein forming the epitaxial layer comprises forming a polysilicon layer.

60. (original) The method of claim 57 wherein forming the third functional element comprises forming an I/O controller, memory, FPGA, or microprocessor.

61. (new) A programmable array module comprising:

at least a first integrated circuit functional element including a field programmable gate array; and

at least a second integrated circuit functional element including a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit functional element,

wherein said field programmable gate array is programmable as a processing element, and wherein said memory array is functional to accelerate external memory references to said processing element.

62. (new) A programmable array module comprising:

at least a first integrated circuit functional element including a field programmable gate array; and

at least a second integrated circuit functional element including a memory array stacked with and electrically coupled to said field programmable gate array of said first integrated circuit functional element, said first and second integrated circuit functional elements being coupled by a number of contact points distributed throughout the surfaces of said functional elements,

wherein said field programmable gate array is programmable as a processing element, and wherein said memory array is functional to accelerate external memory references to said processing element.

63. (new) The programmable array module of claim 62 wherein said contact points are further functional to provide test stimulus from said field programmable gate array to said at least second integrated circuit functional element.

64. (new) The programmable array module of claim 62 further comprising:

at least a third integrated circuit functional element stacked with and electrically coupled to at least one of said first or second integrated circuit functional elements.

65. (new) The programmable array module of claim 64 wherein said third integrated circuit functional element includes another field programmable gate array.

66. (new) The programmable array module of claim 64 wherein said third integrated circuit functional element includes an I/O controller.

67. (new) A method of fabricating a processor module comprising:

forming at least a first integrated circuit functional element such as a microprocessor on a base wafer;

using wafer processing techniques, forming at least a second integrated circuit functional element such as a field programmable gate array on the first integrated circuit functional element; and

forming a third functional element integrated with the first two functional elements using wafer processing techniques,

wherein forming the third functional element comprises forming an epitaxial layer.

68. (new) The method of claim 67 further comprising forming an electrical contact between at least one of a plurality of metal pads associated with the first integrated circuit functional element and at least one of a plurality of metal pads associated with the second integrated circuit functional element.

69. (new) The method of claim 67 wherein forming the second integrated circuit functional element comprises forming an epitaxial layer.

70. (new) The method of claim 69 wherein forming the epitaxial layer comprises forming a polysilicon layer.

71. (new) The method of claim 67 further comprising forming a silicon dioxide layer on a top surface of the first integrated circuit functional element.

72. (new) The method of claim 67 further comprising etching through the second integrated circuit functional element so that an electrical interconnection can be established between the first and second integrated circuit functional elements.

73. (new) The method of claim 67 wherein forming the epitaxial layer comprises forming a polysilicon layer.

74. (new) The method of claim 67 wherein forming the third functional element comprises forming an I/O controller, memory, FPGA, or microprocessor.